In the claims:

Please amend the claims as follows:

Claim 1. (Currently Amended) A memory controller hub comprising:

an internal graphics subsystem adapted to perform graphics operations on data; and

a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and available to an external graphics controller coupled to the memory controller hub to store graphics data.

Claim 2. (Currently Amended) The memory controller hub of claim 1 further including a dedicated bus interface coupling the external graphics controller to the memory controller hub.

Claim 3. (Original) The memory controller hub of claim 2 wherein the dedicated bus interface includes an accelerated graphics port (AGP).

Claim 4. (Currently Amended) The memory controller hub of claim 1 configured to provide a block of linear, virtual memory addresses for use by the internal graphics subsystem, wherein the cache is adapted to store addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 5. (Currently Amended) The memory controller hub of claim 1 configured to provide a block of linear, virtual memory addresses for use by the external graphics controller, wherein the cache is adapted to store addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 6. (Currently Amended) The memory controller hub of claim 1 configured to provide a first block of linear, virtual memory addresses for use by the external graphics controller and adapted to provide a second block of linear, virtual memory addresses for use by the internal graphics subsystem, wherein the cache is adapted to store addresses of locations in

physical memory that correspond to addresses within the first block of linear, virtual memory addresses and to store addresses of locations in physical memory that correspond to addresses within the second block of linear, virtual memory addresses.

Claim 7. (Currently Amended) A computer system comprising:

a CPU;

a display device;

a system memory adapted to store video data and non-video data; and

a memory controller hub coupled to the CPU and coupled to the system memory, the memory controller hub comprising:

an internal graphics subsystem configured to perform graphics operations on graphics data; and

a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and that available to an external graphics controller coupled to the memory controller hub to store graphics data.

Claim 8. (Currently Amended) The computer system of claim 7 further including a dedicated bus interface coupling the external graphics controller to the memory controller hub.

Claim 9. (Original) The computer system of claim 8 wherein the dedicated bus interface includes an accelerated graphics port (AGP).

Claim 10. (Currently Amended) The computer system of claim 7 wherein the memory controller hub is configured to provide a block of linear, virtual memory addresses for use by the internal graphics subsystem; and

wherein the cache is adapted to store addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 11. (Currently Amended) The computer system of claim 7 wherein the memory controller hub is configured to provide a block of linear, virtual memory addresses for

use by the external graphics controller; and

wherein the cache is adapted to store addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 12. (Currently Amended) The computer system of claim 7 wherein the memory controller hub is configured to provide a first block of linear, virtual memory addresses for use by the external graphics controller and is adapted to provide a second block of linear, virtual memory addresses for use by the internal graphics subsystem; and

wherein the cache is adapted to store addresses of locations in physical memory that correspond to addresses within the first block of linear, virtual memory addresses and is adapted to store addresses of locations in physical memory that correspond to addresses within the second block of linear, virtual memory addresses.

Claim 13. (Currently Amended) A method of storing addresses of locations in physical in a memory controller hub cache wherein the locations in physical memory are available to either an external graphics controller coupled to the memory controller hub or are available to an internal graphics subsystem of the memory controller hub.

Claim 14. (Currently Amended) The method of claim 13 further comprising:

providing a block of linear, virtual memory addresses the memory controller hub for use by the internal graphics subsystem; and

storing in the cache addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 15. (Currently Amended) The method of claim 13 further comprising:

providing a block of linear, virtual memory addresses in the memory controller hub for use by the external graphics controller; and

storing in the cache addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.

Claim 16. (Currently Amended) The method of claim 13 further comprising:

providing a block of linear, virtual memory address the memory controller hub for use by the external graphics controller, and storing in the cache addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses; or

providing a block of linear, virtual memory address the memory controller hub for use by the internal graphics subsystem, and storing in the cache addresses of locations in physical memory that correspond to addresses within the block of linear, virtual memory addresses.